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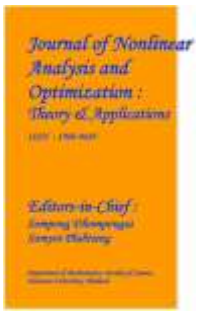

CONSTRUCTION OF LOW POWER, IMPROVED WRITE ABILITY SRAM FOR SPACE APPLICATIONS

[1]Prathap Kumar M, [2]Neelima Gottimukkala, [3]Pinapati Ravi Kumar, [4]Borelli Prathap
[1,2,3]Assistant Professor, [4]Student, Dept. of Electronics & Communication Engineering, Newton's Institute of Engineering, Macherla, Andhra Pradesh, India.

ABSTRACT
SRAM(Static Random Access Memory) Cell for advanced space applications must achieve high performance to meet the ever increasing data rates of space systems and must be radiation hardened to ensure reliable operation in harsh environment. The operation of the SRAM memory cell is relatively straight forward. Access to the SRAM cell is enabled by the Word Line(WL). This controls the two access control transistors which control whether the cell should be connected to the Bit Lines(BL).These two lines are used to transfer data for both read and write operations. There are three modes of operations in SRAM cell. SRAM cell often need to be less power power hungry and should have enhanced performance.So, a new SRAM cell is proposed which has higher critical charge and lower write delay/power.The proposed DWA12T SRAM cell has lower enhanced critical charge which makes it suitable for space applications. All designs were implemented using Hspice in 16nm technology for varying supply voltages.
KEYWORDS: SRAM, Stability, Write delay, Read delay, Low leakage power, Soft error issue.

I. INTRODUCTION

The applications of satellite communication are ubiquitous. From weather forecasting to navigation systems, military surveillance to television, the benefits that the modern world reaps from satellites are endless. With an improvement in technology, there is an inclination toward building lowcost and lightweight satellites [1]. This is because the greater the mass, the greater the cost involved in manufacturing, launching, and maintaining it in space, all of which must be recovered through communication sales over the lifetime of the satellite. Due to the limited resources that a low-cost satellite can be equipped with, there is a major demand for high-density memory devices that are capable of withstanding harsh space radiations with long battery lives [2]. SRAM cells, due to their high packaging density and the ability to provide improved logic performance, are a reasonable choice for space applications [3], [4]. The most effective way of curtailing power dissipation to lengthen battery life in SRAM cells is by downscaling of supply voltage (VDD). This is because standby power reduces exponentially and dynamic power reduces quadratically with VDD [5].

This, however, leads to a plethora of problems. The SRAM cell becomes more susceptible to soft errors, being it in the form of single-cell upsets (SCUs), where a single bit of data is affected, or multiple-cell upsets (MCUs), where multiple bits of data are affected, as supply voltage is decreased. This is because the critical charge Qc, which is defined as the minimum amount of charge required to flip the stored data in an SRAM cell when subjected to space radiations such as high-energy α particles, reduces with V DD [5]. Moreover, the chances of threshold voltage (Vt) mismatch between the adjacent transistors in a memory cell increase as technology advances toward deep sub-micrometer (DSM) due to line edge roughness (LER) and random dopant fluctuation (RDF) [6]. In addition, the probability of read upset and write failure also rises due to the inability of the conventional 6T SRAM cell to maintain the required device strength ratio as the effect of

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process, voltage, and temperature (PVT) variations becomes more prominent with (V_{DD}) scaling [7]. The conventional 6T also suffers from half-select disturbance, which may lead to miswriting in the unselected cells.

II. STATIC RAM:

SRAM (Static Random Access Memory) is a type of Random Access Memory (RAM) that uses latches to store each bit.

A typical SRAM cell is made up of six MOSFETs, and is often called a 6T SRAM cell.

6T SRAM is the conventional SRAM design. This is made up of six transistors, whereby two of the transistors are PMOS.

The configuration is such that the PMOS and NMOS form a cross-coupled inverter while two NMOS transistors are connected one each to the bit lines.

Thus, these NMOS bit lines connected transistors are referred to as the "access transistors" which are controlled by the word line.

III.HSPICE TOOL IMPLEMENTATION:

Install the software H-spice with latest version.After installing, generate the license in LM tools to run our code.Open the notepad and write a code for circuit(called netlist code). Save this file as "filename.sp" format.Open H-spice software and browse the path of the netlist code file.Click "simulate" to simulate the circuit and H-spice will start running our code.Click "Edit LL" to view our output. This file contains all the information about measurement results, operating points and error messages.Once it is verified there is no error messages, click "waveview".H-spice will start viewing the circuit waveforms.

IV.6T SRAM CELL:

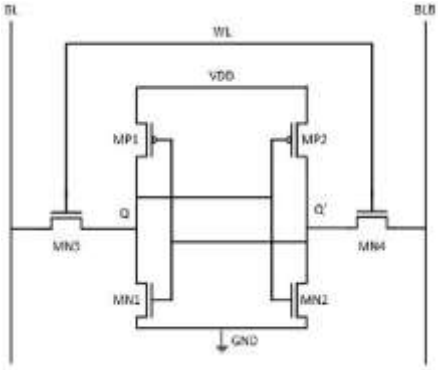

Fig-1: 6T SRAM CELL

READ OPERATION:

This is the state when data is requested from the memory cell. Thus, to read data, both bit line (BL) and bit line-bar (BLB) are initially pre-charged to a logic state 1 (Vdd), when the word line (WL=0) is low.After the pre-charge cycle the word line (WL) is enabled (WL=1) thus the access transistors (MN3 and MN4) are switched ON thereby connecting them to the bit lines.

WRITE OPERATION:

This is the state when data is written/updated in the cell.To write data into a cell, the sense amplifier and pre-charge circuits are deactivated while write enable and the word line are first activated then the input data is driven through the write driver input pin then the bit line is pulled to the value of the given data while the bit line bar (BLB) takes the complementary value. For instance, if data=0 then BL =0 while BLB = 1 (Vdd); whereas, if data=1 then BL =1(Vdd) while BLB = 0 (gnd).Hence, given that transistors MP1 and MN3 are correctly sized then cell will flip and the data is effectively written. Vdd.

HOLD OPERATION:

This is the state when the SRAM cell is idle (data is held in latch) and the bit line and bit line bar are kept at gnd when the access transistors are disconnected because the word line is not inserted.Thus, the PMOS transistors will continue to reenforce each other as long as they are connected to the power supply in order to

keep the data stored in the latch.Also from figure 1a, during this idle/retention mode, when "1" is stored in the cell, MP1 and MN1 are ON hence there exists a positive feedback between Q and QB nodes making Q to be pulled to Vdd.Similarly, when "0" is stored in the cell, MP1 and MN1 are OFF while QB is pulled to Vdd.

V.RELATED WORKS:

The fully differential 8T(FD8T) makes use of decoupling inverter to reduce the Half-Select disturbance, but it also results in degradation of read stability (RSNM).

The improvements in Qcis obtained by single-ended disturb free 9T, which employs single ended decoupled reading technique to isolate their stored nodes from bit-lines during reading operation.

This results data-dependent bit line leakage. The Bit-interleaving architecture-implementing 9T reduce the static power dissipation. However, their hold stability is highly degraded. The differential 12T (D12T) introduces a data-dependent leakage control system to restrict the static power dissipation.

Though it improves the read stability, the leakage power of WWL12T is considerably High. In order to optimize both read stability and write ability along with low leakage power dissipation, half-select free dynamic loop-cutting write assist 12T (DWA12T) SRAM is proposed. This paper will propose a power efficient new SRAM (Static Random Access Memory) Cell for satellites to extend the battery life of memory cells.

This New SRAM cell is assumed to achieve a furthermore lower write delay, read delay and higher the stabilities of read, write and hold modes of operation, to mitigate the soft error issues, compared to that of previously proposed FED8T/9T/D12T/DWA12T under severe process and various temperature conditions.

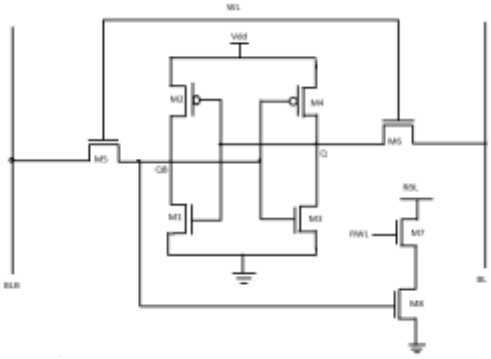

Fig-2: 8T SRAM CELL

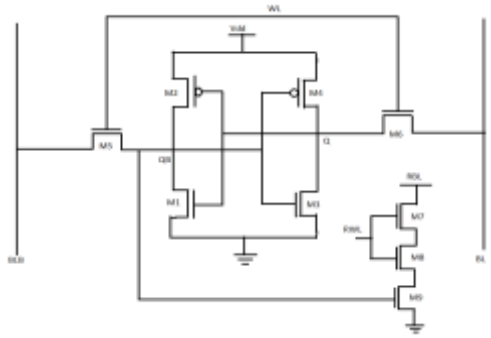

Fig-3: 9T SRAM CELL

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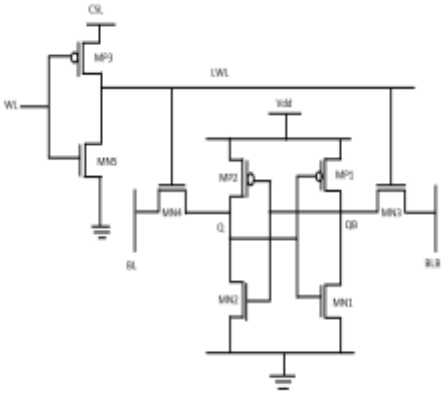

Fig-4: FD8T SRAM CELL

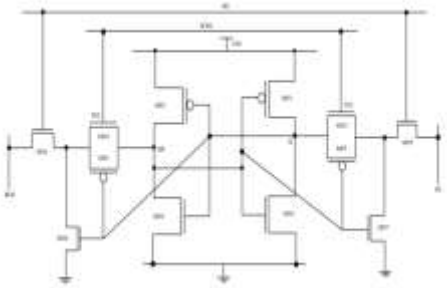

Fig-5: WWL12T SRAM CELL

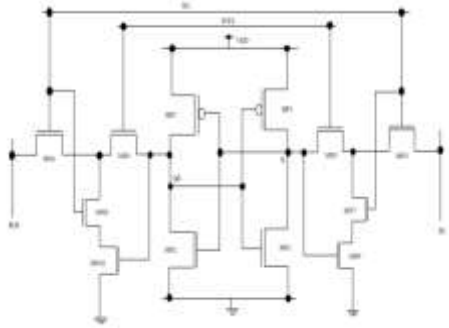

Fig-6: D12T SRAM CELL

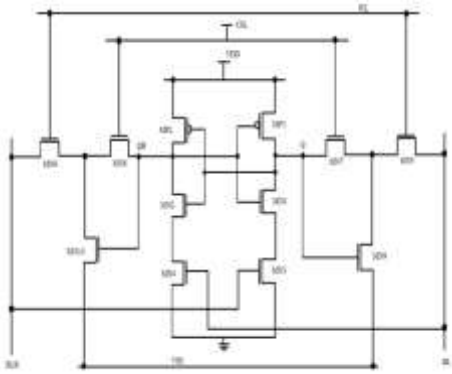

Fig-7: DWA12T SRAM CELL

VI. PROPOSED DWA12T (PDWA12T) SRAM cell:

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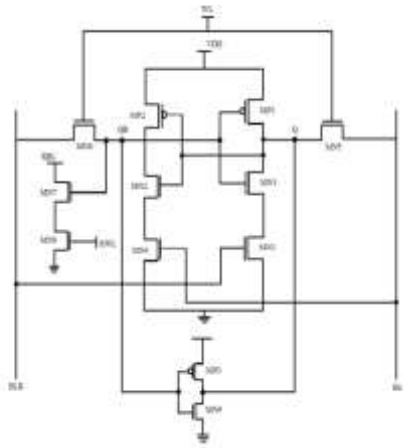

Fig-8: PDWA12T SRAM CELL

The schematic circuit diagram of the proposed DWA12T is shown below in fig.(8). The word line(WL) activates the access transistors MN5 and MN6, which is controlled by the bit lines BL and BLB. One additional CMOS inverter is placed in between the storage nodes Q and QB. Additional two NMOS transistors, MN3/MN4, is connected in series with pull-down transistors, MN1/MN2, and is controlled by BLB/BL. The other two transistors MN7/MN8 is accessed by separate control signals RWL/RBL, which is connected at storage node QB.

Write operation:

The word line(WL) have to be active in write operation such that the access transistors MN5 & MN6 will be ON. Depends on either '1'/'0' or '0'/'1' is to be written to storage node 'Q'/'QB', the bit lines BL/BLB is either kept at VDD/GND or GND/VDD. Let's assume the case Write-1 i.e, '1' is to be written to the storage node Q. In this case, BL is at VDD and BLB is at GND, so the dynamic loop-cutting transistor MN3 is off and MN4 is on. As MN3 is off, there is no path to the GND at the right side. This causes the reduction in pull-down strength and increases the pull-up strength. But the pull-down strength at the left side remains same. As the pull-up strength increases, it becomes easier to write '1' into the storage node 'Q', in turn, quickens the write operation. This process is vice-versa for write-0 operation.

Read operation:

In this Proposed DWA12T SRAM cell, there is separate bit line and word line i.e, RBL and RWL. Before performing the read operation, firstly pre-charge the bit line RBL to high (VDD). The word line, RWL, is to be kept at high (VDD) inorder to activate the transistor MN8. Also inactivated the control signals WL and BL/BLB. Depends on either 'Q'/'QB' stores the data '1'/'0', either RBL or BL/BLB discharges to the ground. Let's assume the case Read-0 operation i.e, the data '0' is to be read from the storage node 'Q'. As 'Q' is '0', 'QB' will be '1'. Also, RWL and RBL is kept at high, there is a discharging path through the transistors MN7, MN8 to the GND. There is a sense amplifier(not shown) connected in between the bit lines, which identifies the voltage difference between them. Thus, completes the read-0 operation. This process is vice-versa for read-1 operation.

Hold operation:

During the hold operation, all the access transistors are turned off by making the word line (WL) , RBL, RWL to GND. The bit lines BL and BLB are to be kept at high, such that the driver transistors are only present, also the loop-cutting transistors MN3 and MN4 are in on position. Thus, the stored data will be retained in hold operation.

	Write(0 or 1)	Hold	Read
WL	0	1	0

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RBL	1	0	1
RWL	1	0	1
BL	0/1	1	1
BLB	1/0	1	1

Fig-9: Proposed DWA12T Truth table

Dynamic Loop-Cutting Write Assist Mechanism:

The write operation begins with CSL and WL being set to V_{DD}. VSS is kept at V_{DD}. Depending on whether "1" ("0") or "0" ("1") is to be written to storage node "H" ("L"), BL/BLB is either kept at V_{DD}/GND or GND/V_{DD}. Let us consider the case in which "1" is to be written to "0" storing node "H." Since BL/BLB is at V_{DD}/GND in this case, the dynamic loop-cutting transistor MN3/MN4 is turned off/on. As MN3 is off, the right-hand side core inverter is disconnected from GND. This reduces the pull-down strength of the inverter while enhancing its pull-up strength, which, in turn, increases the ease with which "1" can be written to "H." On the other hand, the pull-down strength of the left-hand side core inverter remains intact. Initially, the writing process is hampered by the additional charging path from VSS (kept at V_{DD}) as the "1" storing node "L" turns MN10 on for a brief time. However, as the voltage at "L" falls, MN10 is turned off. On the other hand, MN9 is initially turned off by "0" storing node "H." However, as the voltage at "H" rises, it turns MN9 on and an additional charging path from VSS (kept at V_{DD}) is established via MN9 and MN7, which, in turn, quickens the write operation. This completes the write "1" operation. Therefore, the effect of an unwanted additional charging path is nullified by that of an advantageous additional charging path, rendering the dynamic loop-cutting technique as the chief writing mechanism. A similar process occurs while writing "0".

Decoupled Differential Read Technique:

At the beginning of the read operation, both BL and BLB are pre-charged high, while VSS is set at GND. WL is kept at V_{DD} to activate MN5 and MN6. CSL is kept at GND to isolate the storage node "H"/"L" from BL/BLB. Depending on whether "H" ("L") stores "1" ("0") or "0" ("1"), either BL or BLB discharges through read buffer MN9 or MN10 to GND. The bitlines are connected to the inputs of a sense amplifier (not shown), which detects a 50-mV voltage difference between them and completes the read operation.

VII.SIMULATION SETUP AND RESULTS:

The 16-nm CMOS predictive technology model (PTM) [19] and HSPICE have been utilized for the analysis of major design metrics of the proposed DWA12T cell. In order to estimate its relative performance, the proposed cell has been compared with other contemporary designs, such as the 6T,8T,FD8T ,9T, WWL12T, D12T, DWA12T cells. Given that transistor sizing is a crucial factor that determines behaviour of SRAM cells, all cells have been assigned appropriate sizings. Since process variation is severe in the DSM technology node, its impact has been considered by employing the same simulation.

WRITE DELAY:

The write delay or write access time for writing "1" to "0" storing node "H" is estimated, as specified in [17]. From which shows TWA of different comparison cells at various V_{DD}, it is evident that the DWA12T cell exhibits the longest Write ability. This is due to the application of an additional column-decoupling nMOS, MN9, to drive the LWL from WL, which reduces the LWL swing and, consequently, weakens the driving strength of its access transistors [5]. Writing "1" to the 9T cell is rather difficult due to its single-ended asymmetrical writing scheme, which leads to a significantly longer T_{WA} than that of other differential writing cells. The WWL12T cell exhibits longer write delay than DWA12T and D12T cells due to the presence of additional TGs in its access path, which refreshes the data stored in its storage nodes and slows down the write operation. The proposed DWA12T cell exhibits considerably shorter TWA than D12T due to the use of

dynamic loop-cutting writing scheme. However, in the absence of series-connected access transistors in its access path, the FD8T cell exhibits a 1.37× shorter TWA than the proposed design.

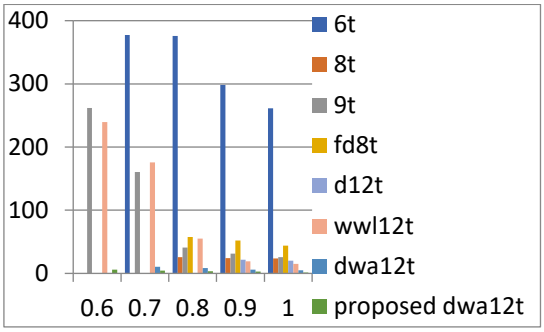

Fig-10: Write-1 Delay bar graph

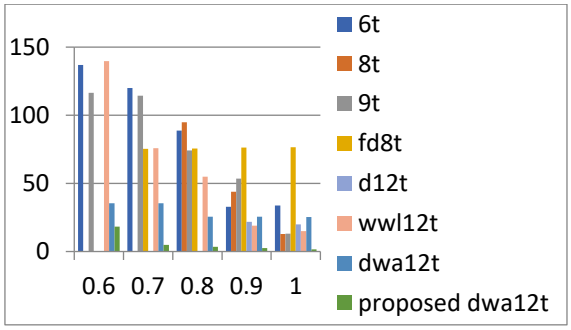

Fig-11: Write-0 Delay bar graph

READ DELAY:

For cells with dual-bitline structures, read access time (T_{RA}) is estimated as the time required to reach 50-mV voltage difference between the two bitlines after the activation of WL whereas for fair comparison, T_{RA} of single-ended reading cells is estimated as the time required to discharge the bitline by 50 mV from its initial pre-charged value (V_{DD}) after the activation of WL. It can includes T_{RA} of different comparison cells at various V_{DD}values, that the 8T shows the longest T_{RA} because of the increase in overall bitline capacitance due to the sharing of bitlines by both, access transistors and read buffers. The 9T and D12T cells exhibit similar T_{RA} as their read paths are equivalent. Since DWA12T and WWL12T have the same read path, which consists of two transistors in their read path when compared to three read transistors in that of 9T/D12T cell, they show shorter T_{RA} than 9T/D12T. Due to its 6T like structure and optimum β ratio, FD8T shows the shortest T_{RA}.

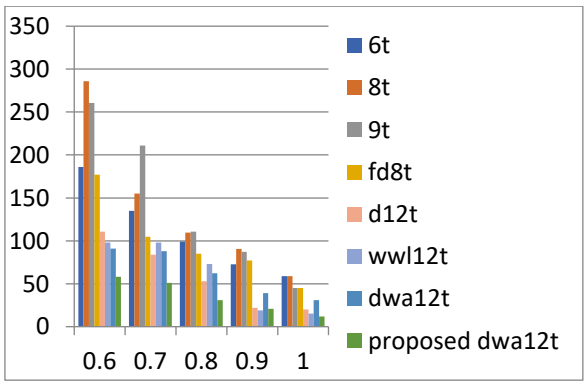

Fig-12: Read Delay bar graph

AVERAGE POWER :

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In the modern technology power consumption is the main criteria to utilization of the less power in the modern technology is required. In the normal 6T SRAM the word line used only w but, in this we are using the two word lines w1 and w2 to make the better results.

The Average power is decreased from the Basic SRAM to the improved SRAM is 90 % and the 8T SRAM to the improved SRAM is 21%. So, we can use this method interim of power utilization and better SNM of the circuit. By increasing scaling we can even reduces the powerconsumption and able to increases the wide applications for this circuit. Accordingly,it is possible to achieve less Average power from the Basic circuit by making inactive unused part.

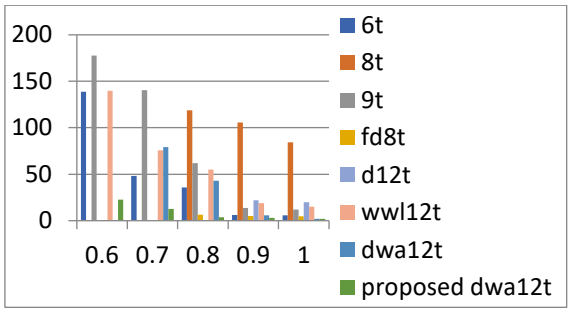

Fig-13: Write-1 Average Power bar graph

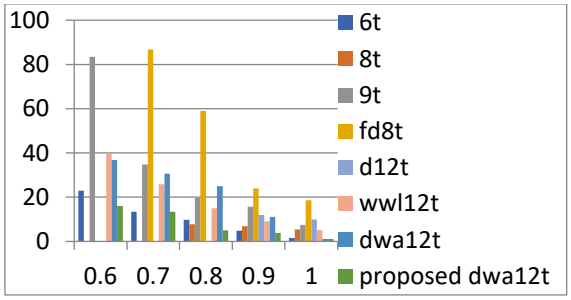

Fig-14: Write-0 Average Power bar graph

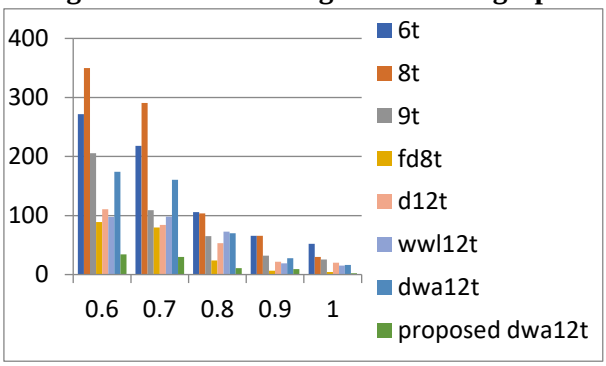

Fig-15: Read Average Power bar graph

CRITICAL CHARGE:

An SRAM cell operating in space is highly susceptible to soft errors. As explained earlier in Section I, the minimum amount of charge needed to reverse the data stored in a cell and produce a soft error is known as the critical charge (Qc). Given that the rate of occurrence of soft error (SER) is exponentially dependent on Qc, Qc of an SRAM cell is higher and its susceptibility to soft errors is lower.Nflux is the neutron flux intensity, A is the crosssectional area of the storage node affected by radiation, and Qs is the efficiency with which the device collects the charges. Since Qs is generally in fC, a marginal increase in Qc leads to a significant reduction in SER. In order to study the impact of space radiation on the proposed cell, we have estimated Qc of DWA12T and compared it with that of the FD8T SRAM cell, through SPICE-based simulations using doubleexponential current source model.

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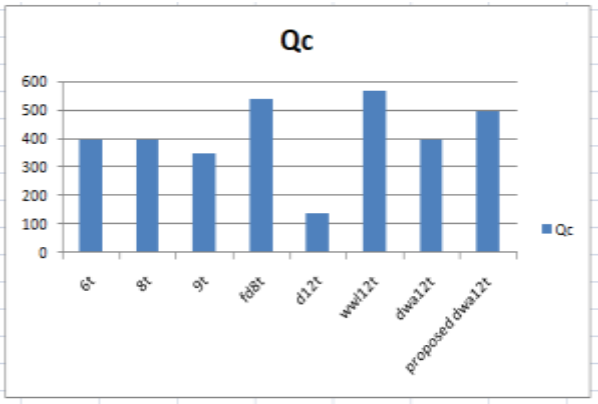

Fig-16: Critical Charge bar graph

COMPARISION TABLE:

	Read Delay (innsec)	Write-0 Delay (innsec)	Write-1 Delay (innsec)	Read Average Power (innWatt)	Write-0 Average Power (innWatt)	Write-1 Average Power (innWatt)	Critical Charge (in ac)
6T SRAM	58.932	33.767	261.496	51.9776	1.57588	5.67687	395.5588
8T SRAM	58.932	12.8776	23.58	29.97868	5.50001	84.46	395.9707
9TSRAM	45.092	13.012	25.969	25.6031	7.4452	11.898	346.0588
FD8T SRAM	45.092	76.4654	43.757	4.2339	18.673	4.7654	537.4925
WWL12T SRAM	15.087	15.087	15.087	15.087	5.087	15.087	568.5504
D12T SRAM	19.966	19.966	19.966	19.966	9.966	19.966	137.6932
DWA12T SRAM	31.032	25.2628	4.7866	16.075	1.0533	1.8786	397.0098
PROPOSED DWA12T SRAM	12.0272	1.51487	1.2717	2.4225	1.086	1.8776	495.902

CONCLUSION

A reliable, low-power, half-select free DWA12T SRAM cell has been proposed in this article. The proposed cell exhibits considerable improvement in write ability and write delay due to the application of dynamic loop-cutting write assist mechanism. The read stability is significantly enhanced due to the use of decoupled

differential-read mechanism. The DWA12T cell exhibits very low static power dissipation as VSS is kept at V DD during the standby mode to curtail bit line leakage, while the presence of additional dynamic loop-cutting transistors in the core cell increases the effective channel length and reduces the flow of leakage current. Even when subjected to harsh cosmic radiations in space, the proposed cell exhibits relatively low susceptibility to soft error. Moreover, its half-select disturb-free nature renders it capable of implementing the bit-interleaving architecture and, thus, compatible with the application of appropriate ECCs. Thus, the DWA12T is an optimum choice for power-efficient and reliable cache memory design for cost-effective lightweight satellite applications.

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